HCNR4904

40V N-Channel MOSFET

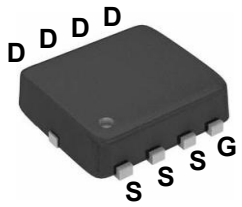
General Description

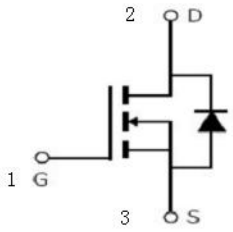
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	40V
I_D (at V_{GS}=10V)	70A
$R_{DS(ON)}$ (at V_{GS}=10V)	4.2mΩ(Typ)

PDFN3*3





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	TC=25°C	I_D	70	A
	TC=100°C	I_D	44	A
Maximum Power Dissipation		P_D	52	W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		1.1	℃ /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		62	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=20A		4.2	5.5	mΩ
		V_{GS}=4.5V, I_D=10A		5.3	7.0	mΩ
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		2400		pF
C_{oss}	Output Capacitance			230		pF
C_{rss}	Reverse Transfer Capacitance			150		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=20V,I_D=1A, V_{GS}=10V, R_G=3.3Ω		14		nS
t_r	Turn-on Rise Time			18		nS
$t_{d(off)}$	Turn-Off Delay Time			38		nS
t_f	Turn-Off Fall Time			14		nS
Q_g	Total Gate Charge	V_{DS}=30V,I_D=10A, V_{GS}=4.5V		25		nC
Q_{gs}	Gate-Source Charge			6.5		nC
Q_{gd}	Gate-Drain Charge			12		nC
V_{SD}	Diode Forward Voltage (2)	V_{GS}=0V,I_{SD}=1A		0.72	1.3	V
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz		1.6		Ω

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

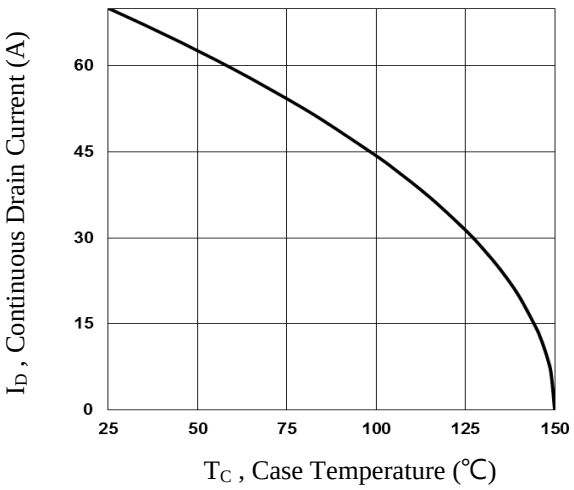


Fig.1 Continuous Drain Current vs. T_C

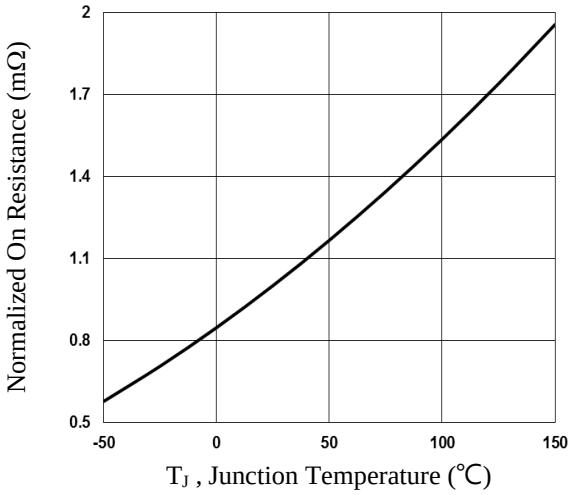


Fig.2 Normalized RDSON vs. T_J

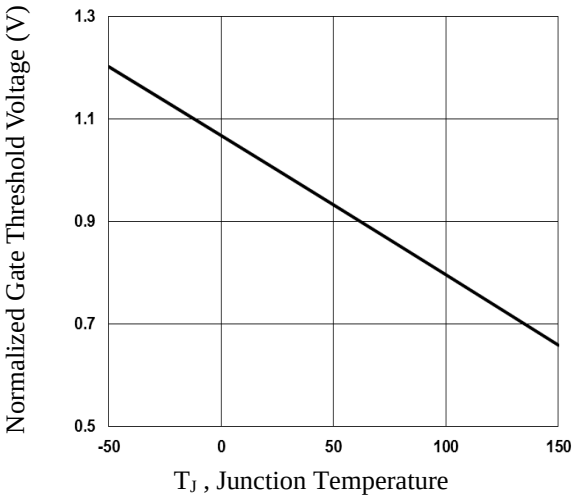


Fig.3 (℃) Normalized V_{th} vs. T_J

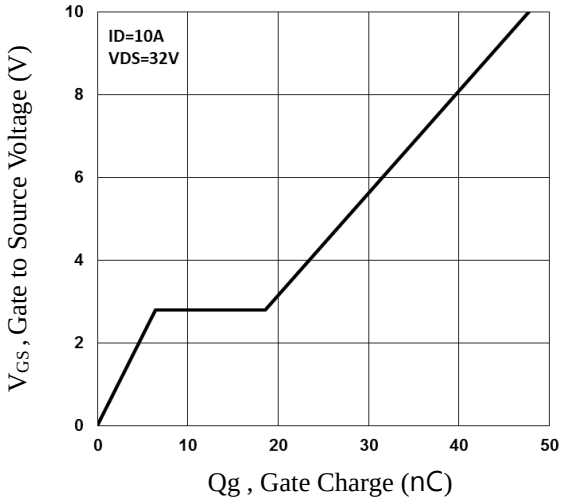


Fig.4 Gate Charge Waveform

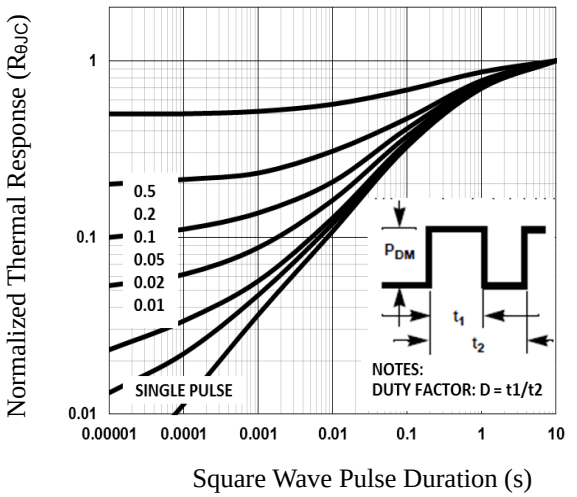


Fig.5 Normalized Transient Impedance

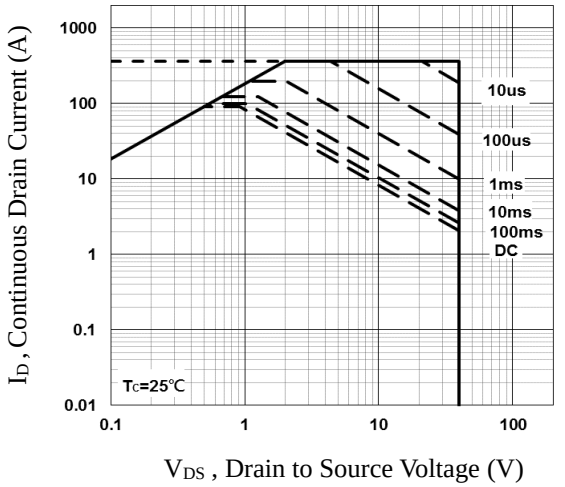


Fig.6 Maximum Safe Operation Area

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

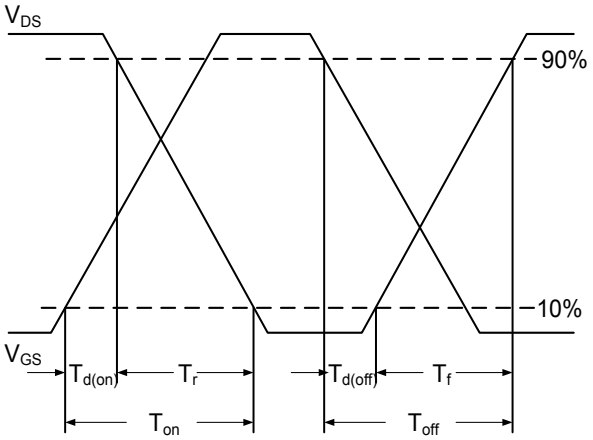


Fig.7 Switching Time Waveform

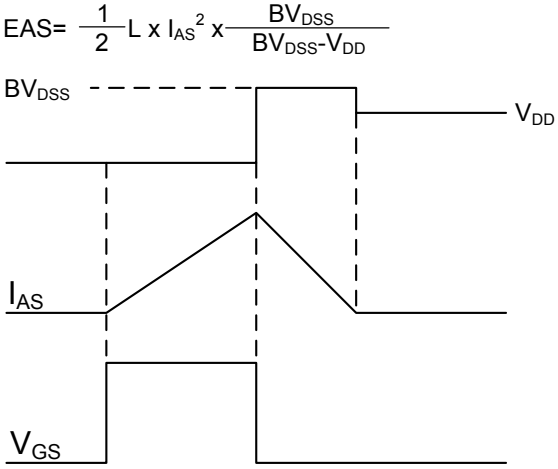
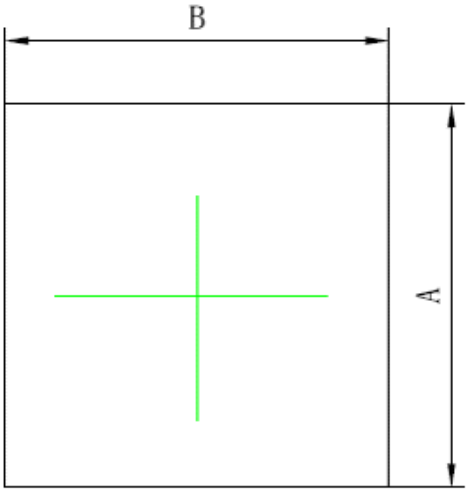
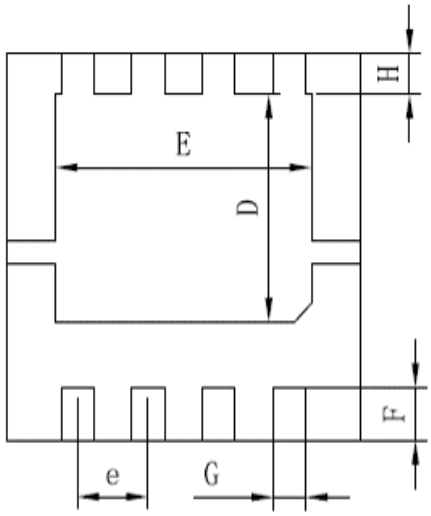
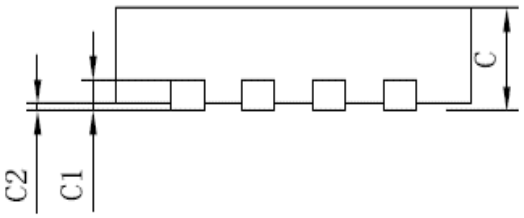


Fig.8 EAS Waveform

DFN3.3X3.3 PACKAGE INFORMATION







A	B	C	C1
3.25±0.05	3.25±0.05	0.8±0.05	0.2±0.02
C2	D	E	F
0.05Max	1.9±0.1	2.35±0.15	0.45±0.05
G	H	e	
0.3±0.05	0.35±0.05	0.65±0.05	
单位：mm			